CLAIM AMENDMENTS

IN THE CLAIMS

This listing of the claims will replace all prior versions, and listing, of claims in the application or previous response to office action:

1. **(Currently Amended)** An **apparatus** ~~**information handling system**~~, comprising:

~~**memory;**~~

~~**at least one processor operably associated with the memory;**~~

a printed circuit board **(PCB)** ~~**operable to maintain the processor and the memory**~~;

a ~~**plurality of vias**~~ **via** disposed in at least ~~**one printed circuit board**~~ **a first** layer **of the PCB**, the ~~**vias**~~ **via** defined by a first opening on a first surface of the ~~**printed circuit board**~~ **first** layer, a second opening at a second surface of the ~~**printed circuit board**~~ **first** layer and at least one side wall connecting the first and second openings and defining a void therebetween; and

a conductive material disposed on a portion of the side wall, the conductive material defining ~~**at least one**~~ **a set of at least one** inner-via trace**:**

wherein the via terminates proximate a first surface of a second layer of the PCB wherein the first surface of the second layer comprises an internal surface disposed between the second layer and an adjacent layer.

2. **(Withdrawn)** The information handling system of Claim 1, further comprising the inner-via trace having a total impedance substantially approximating a printed circuit board surface mounted trace impedance.

3. **(Currently amended)** The ~~**information handling system**~~ **apparatus** of Claim 1, further comprising:

the conductive material disposed in the void defining a plurality of inner-via traces, and

the plurality of inner-via traces arranged in a striped pattern, where the patterned stripes travel between the first opening and second opening.

4. **(Currently amended)** The ~~**information handling system**~~ **apparatus** of Claim 1, further comprising a conductive pad disposed on the first surface of the printed circuit board layer and proximate the first opening and coupled to the inner-via traces.

5. **(Currently amended)** The ~~**information handling system**~~ **apparatus** of Claim 4, further comprising a conductive pad disposed on the second surface of the printed circuit board layer and proximate the second opening and coupled to the inner-via traces.

6. **(Currently amended)** The ~~**information handling system**~~ **apparatus** of Claim 1, further comprising a conductive trace disposed on the first surface of the printed circuit board layer and coupled to the inner-via traces.

7. **(Currently amended)** The ~~**information handling system**~~ **apparatus** of Claim 6, further comprising a conductive trace disposed on the second surface of the printed circuit board layer and coupled to the inner-via traces.

8-14. (Canceled).

15. (Withdrawn) An apparatus, comprising:
at least one substrate having a first surface and a second surface;
a first conductive trace disposed proximate the first surface of the substrate;
a second conductive trace disposed proximate the second surface of the substrate;
at least one a via disposed in the substrate, the via defining an aperture in the substrate traveling from the first surface to the second surface; and
at least one conductive inner-via trace operably coupled to the via, the inner-via trace operably coupling the first conductive trace to the second conductive trace and having at least one electrical characteristic substantially approximating a corresponding electrical characteristic of a substrate surface conductive trace.

16. (Withdrawn) The apparatus of Claim 15, further comprising the inner-via trace having an impedance measure substantially approximating an impedance measure of the first and second conductive surface traces.

17. (Withdrawn) The apparatus of Claim 15, further comprising:
the substrate having a plurality of layers; and
the first conductive trace disposed between a first pair of substrate layers and the second conductive trace disposed between a second pair of substrate layers.

18. (Withdrawn) The apparatus of Claim 15, further comprising:
the substrate having a first plurality of layers; and
the first conductive trace disposed on an external surface of the plurality of substrates and the second conductive trace disposed between adjacent layers of the plurality of substrates.

19. (Withdrawn) The apparatus of Claim 15, further comprising:
a plurality of conductive inner-via traces; and
the plurality of conductive inner-via traces collectively having at least one electrical characteristic substantially approximating a corresponding electrical characteristic of a substrate surface conductive trace.

20. (Withdrawn) The apparatus of Claim 19, further comprising an impedance total for the plurality of inner-via traces substantially approximating that of the first surface conductive trace and the second surface conductive trace.

21. **(New)** The apparatus of Claim 1, wherein the first surface of the first layer comprises an internal surface disposed between the first layer and an adjacent layer.

22. **(New)** The apparatus of Claim 1, further comprising the set of at least one inner-via trace having a total impedance substantially approximating a printed circuit board surface mounted trace impedance.